GUDLAVALLERU ENGINEERING COLLEGE

(An Autonomous Institute with Permanent Affiliation to JNTUK, Kakinada)
Seshadri Rao Knowledge Village
Gudlavalleru – 521 356, Krishna District, Andhra Pradesh
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The **12th** Meeting of **Academic Council** of Gudlavalleru Engineering College (Autonomous), Seshadri Rao Knowledge Village, Gudlavalleru is held today i.e. 28-07-2019 (Sunday) at 10-30 AM in the Management's Conference Hall of the college under the Chairmanship of Dr. P. Ravindra Babu, Principal of the College.

MEMBERS PRESENT:

Sl. No.	Name of the Member	Designation	Signature
1	**Dr. P. Ravindra Babu** Principal	Chairman	
2	**Dr. P. Kodanda Rama Rao** Professor & HoD of CE	Member	
3	**Dr. L. Ravi Srinivas** Professor & HoD of EEE	Member	
4	**Dr. M. R. Ch. Sastry** Professor & HoD of ME	Member	
5	**Dr. V. V. K. D. V. Prasad** Professor & HoD of ECE	Member	
6	**Dr. S. Narayana** Professor & HoD of CSE	Member	
7	**Dr. Ch. Kavitha** Professor & HoD of IT	Member	
8	**Dr. Ch. Nirmal Chand** Professor & HoD of MBA	Member	
9	**Dr. G. S. Bhaskara Rao** Professor of Mathematics & HoD of BS&H	Member	Could not attend
10	**Dr. M. Vijaya Lakshmi** Associate Professor & HoD of English	Member	Could not attend.
11	**Dr. S. R. K. Reddy** Prof. of CE and Advisor to the Management	Member	
12	**Dr. P. Nageswara Reddy** Professor of ME & Director (AS&A)	Member	
13	**Mr. Md. Rafi Khan** Associate Professor of EEE	Member	
14	**Mr. D. K. Pavan Kumar** Sr.Gr.Asst.Professor in Mathematics	Member	
15	**Dr. K. Lal Kishore** Director, R&D, CVR College of Engg., Hyderabad Former Vice – Chancellor, JNTUA, Ananthapur, Former Rector, JNTUH, Hyderabad	Member	

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16	**Dr. D. V. L. N. Somayajulu** Professor of CSE, NIT, Warrangal and Director, IIIT, Kurnool	Member	
17	**Dr. Parimi S.R.** Professor of Civil Engineering and Structural Engg. Consultant, Vijayawada,	Member	
18	**Dr. Ramanujam Parthasarathy** Professor of English, G3, Sreeja Apartments, Srinivasa Nagar Bank Colony, Vijayawada.	Member	
19	**Mr. J. S. R. K. Prasad** CEO, Better Castings Pvt. Limited, JRD Tata Industrial Estate, Gantivari Street, Christurajupuram, Kanuru, Vijayawada – 520 007.	Member	
20	**Dr. G. Yesuratnam** Professor of CE, UCEK and Director(i/c), Academic & Planning, JNTUK, Kakinada.	Member	
21	**Dr. R. Srinivasa Rao** Professor of EEE and Director of Evaluation, JNTUK, Kakinada.	Member	
22	**Dr. K. Ramu** Professor of CE and Director, BICS & Infrastructure Development & Chief Engineer, JNTUK, Kakinada	Member	
23	**Dr. K. Syam Sundar** Professor of ME & Controller of Examinations	Invitee	
24	**Dr. G. V. S. N. R. V. Prasad** Professor of CSE & Vice Principal – Academics	Member Secretary	

GUDLAVALLERU ENGINEERING COLLEGE

Seshadri Rao Knowledge Village, GUDLAVALLERU – 521 356

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Minutes of the 12th Meeting of the Academic Council held on 28-07-2019, Sunday in the Management Conference Hall.

12.1 To confirm the minutes of the last Meeting of the Academic Council held on 23-03-2019.

Resolution: The Minutes of the 11th Academic Council meeting held on 23-03-2019 have been confirmed.

12.2 To consider and approve and Course Structure and Syllabi of M.Tech course in VLSI Design and Embedded Systems for the academic year 2019-20.

The Member Secretary presented the course structure and syllabi of M.Tech course in VLSI Design and Embedded Systems for the academic year 2019-20 recommended by the Boards of Studies of ECE. The approved course structure and syllabi of VLSI Design and Embedded Systems is given below.

I Semester

Sl. No.	Name of the Course / Laboratory	No.of Hours per Week			No.of Credits
		L	T	P	
1	Linear and Non-Linear Optimization Techniques	3	-	-	3
2	Embedded System Design **	3	-	-	3
3	Advanced Digital Design	3	-	-	3
4	Advanced Microcontrollers	3	-	-	3
5	CMOS VLSI Circuits	3	-	-	3
6	**Professional Elective – I** 1. Testing & Testability of VLSI Circuits 2. VLSI Digital Signal Processing 3. Real Time Operating Systems 4. Embedded Processors	3	-	-	3
7	VLSI Design Lab	-	-	4	2
	Total :	18	**-**	**4**	**20**

II Semester

Sl. No.	Name of the Course / Laboratory	No.of Hours per Week			No.of Credits
		L	T	P	
1	Research Methodologies	3	-	-	3
2	VLSI System Design **	3	-	-	3
3	Hardware and Software Co-Design	3	-	-	3
4	Internet of Things	3	-	-	3
5	**Professional Elective – II** 1. ASIC System Design 2. Advances in VLSI Design 3. Embedded Computing Architectures 4. Advanced Computer Networks	3	-	-	3

6	**Professional Elective – III** 1. System-on-Chip Design 2. VLSI Interconnects 3. RF VLSI Design 4. Advanced Digital Signal Processing	3	-	-	3
7	Internet of Things Lab	-	-	4	2
8	Seminar	-	-	4	2
	Total :	**18**	**-**	**8**	**22**

III Semester

Sl. No.	Name of the Course / Laboratory	No.of Periods per Week			No.of Credits
		L	T	P	
1	Dissertation – Part A	-	-	-	-

IV Semester

Sl. No.	Name of the Course / Laboratory	No.of Periods per Week			No.of Credits
		L	T	P	
1	Dissertation – Part B	-	-	-	**28**
	Total :	-	-	-	**28**

12.3 To discuss the Modalities to initiate the regulations in 2020.

I) UG – B.Tech Program:

The Member Secretary presented the proposed R20 regulations. The following are the suggestions recommended by the members of the council:

- Students joining the four year B.Tech program shall have to earn **160 credits** for the award of Degree and students joining the B.Tech program into the II year 1st semester directly through Lateral Entry (LE) Scheme shall have to earn **160 minus number of I year credits** for the award of B.Tech degree.
- In case of vertical mobility, Students with no backlogs up to III year 1st semester with CGPA not less than 8.0 may register for two professional elective courses offered in IV year 2nd semester in advance i.e. one in III year 2nd semester and another one in IV year 1st semester so as to have exclusive project work during the IV year 2nd semester. Also suggested to observe the number of registrations during the current academic year to take final decision on vertical mobility.
- The number of open electives may be restricted to maximum of three.
- Include Seminar and Employability skills in the course structure in addition to Industrial/Practical training.

II) PG – MBA & M.Tech Program:

R17 Regulations may be followed in R20 also.

12.4 Any other matter with the permission of the chair.

(i) To review the semester end examination results.

The Academic Council reviewed and ratified the Semester End Examinations results of B.Tech, M.Tech and MBA for the academic year 2018-19.

UG - B.Tech – Class of 2019:

Sl. No.	Branch	No.of Students Appeared	No.of Students Graduated in the four year period of study	Success %	Performance					
					Distinction		First Class		Second Class	
					No.	%	No.	%	No.	%
1	CIVIL	202	**180**	**89.11**	113	**55.94**	54	**26.73**	13	**6.44**
2	EEE	202	**185**	**91.58**	130	**64.36**	45	**22.28**	10	**4.95**
3	ME	210	**185**	**88.10**	107	**50.95**	64	**30.48**	14	**6.67**
4	ECE	276	**260**	**94.20**	205	**74.28**	52	**18.84**	3	**1.09**
5	CSE	272	**250**	**91.91**	198	**72.79**	48	**17.65**	4	**1.47**
6	IT	106	**97**	**91.51**	76	**71.70**	21	**19.81**	-	**-**
Total		**1268**	**1157**	**91.25**	**829**	**65.38**	**284**	**22.40**	**44**	**3.47**

PG – MBA Class of 2019:

Sl. No.	Branch	No.of Students Appeared	No.of Students Graduated in the four year period of study	Success %	Performance					
					Distinction		First Class		Second Class	
					No.	%	No.	%	No.	%
1	MBA	91	**88**	**96.70**	39	**42.86**	48	**52.75**	1	**1.10**

2nd Semester Result Analysis:

UG – B.Tech Programs:

I B.Tech 2nd Semester (R17) (2018 Admitted) Regular Examinations, April 2019

Subject	Reg.	App.	Passed	Failed	Reg. Pass %	App. Pass %
Civil Engineering	112	110	64	46	57.14	58.18
Electrical and Electronics Engineering	99	96	63	33	63.64	65.63
Mechanical Engineering	145	140	82	58	56.55	58.57
Electronics and Communication Engineering	229	228	182	46	79.48	79.82
Computer Science and Engineering	235	233	180	53	76.60	77.25
Information Technology	110	108	65	43	59.09	60.19
Overall Pass Percentage	**930**	**915**	**636**	**279**	**68.39**	**69.51**

II B.Tech 2nd Semester (R17) (2017 Admitted) Regular Examinations, April 2019

Subject	Reg.	App.	Passed	Failed	Reg. Pass %	App. Pass %
Civil Engineering	188	187	145	42	77.13	77.54
Electrical and Electronics Engineering	180	176	116	60	64.44	65.91
Mechanical Engineering	190	183	127	56	66.84	69.40
Electronics and Communication Engineering	283	280	214	66	75.62	76.43
Computer Science and Engineering	255	251	202	49	79.22	80.48
Information Technology	106	106	79	27	74.53	74.53
Overall Pass Percentage	**1202**	**1183**	**883**	**300**	**73.46**	**74.64**

III B.Tech 2nd Semester (R14) (2016 Admitted) Regular Examinations, April 2019

Subject	Reg.	App.	Passed	Failed	Reg. Pass %	App. Pass %
Civil Engineering	184	183	154	29	83.70	84.15
Electrical and Electronics Engineering	178	174	119	55	66.85	68.39
Mechanical Engineering	204	197	147	50	72.06	74.62
Electronics and Communication Engineering	278	271	233	38	83.81	85.98
Computer Science and Engineering	256	254	236	18	92.19	92.91
Information Technology	104	103	86	17	82.69	83.50
Overall Pass Percentage	**1204**	**1182**	**975**	**207**	**80.98**	**82.49**

IV B.Tech 2nd Semester (R14) (2015 Admitted) Regular Examinations, April 2019

Subject	Reg.	App.	Passed	Failed	Reg. Pass %	App. Pass %
Civil Engineering	202	201	195	6	96.53	97.01
Electrical and Electronics Engineering	202	202	191	11	94.55	94.55
Mechanical Engineering	210	206	199	7	94.76	96.60
Electronics and Communication Engineering	276	275	269	6	97.46	97.82
Computer Science and Engineering	272	272	269	3	98.90	98.90
Information Technology	106	105	104	1	98.11	99.05
Overall Pass Percentage	**1268**	**1261**	**1227**	**34**	**96.77**	**97.30**

PG – MBA Programs:

MBA Regular Examinations, April / May 2019

Subject	Reg.	App.	Passed	Failed	Reg. Pass %	App. Pass %
II Semester (R17) (2018 Admitted)	**79**	**77**	**72**	**5**	**91.14**	**93.51**
IV Semester (R17) (2017 Admitted)	**91**	**91**	**91**	**0**	**100.00**	**100.00**

(ii) Ratified the substitute subjects for R17 Regulations submitted by the Chair Persons of various Boards of Studies for the academic year 2019-20.

The Member Secretary presented the list of substitute subjects for R17 regulations recommended by the Chairpersons of various Boards of studies. The List of Substitute subjects have been reviewed and approved. The following are the substitute subjects for Re-admitted candidates (i.e. from R14 regulations to R17 Regulations) recommended by the various Boards of Studies for the academic year 2019-20.

S. No	Course as per R17 Regulations	Course studied under R14 Regulations	Substitute course offered
Civil Engineering			
III B.Tech – 1st Semester			
1	Geotechnical Engineering	Geotechnical Engineering-I	Engineer and Society
2	Hydrology and Water Resource Engineering	Water Resource Engineering – I	Elements of Mechanical & Electrical Engineering
III B.Tech – 2nd Semester			
1	Foundation Engineering	Geotechnical Engineering–II	Engineer and Society
2	Design of R.C. Structures	Design & Drawing of R.C. Structures	Elements of Mechanical & Electrical Engineering

Electrical and Electronics Engineering			
III B.Tech – 1st Semester			
1	Electrical Measurements and Instrumentation	Electrical Measurements and Instrumentation	Numerical Methods with Computer Applications
2	Power System - II	Power System - II	Electrical Materials
III B.Tech – 2nd Semester			
1	Power Electronics	Power Electronics	Switchgear and Protection
2	Probability and Fuzzy Mathematics	Fuzzy Mathematics	Numerical Methods with Computer Applications
3	Electrial Measurements and Instrumentation Lab	Electrical Measurements and Instrumentation Lab	Electrical Machines – II Lab
Mechanical Engineering			
III B.Tech – 1st Semester			
1	Computer Aided Machine Drawing Lab	Machine Drawing	Thermal Engineering Lab
III B.Tech – 2nd Semester			
1	Engineering Economics and Accountancy	Managerial Economics and Financial Analysis	Engineering & Society
			Computer Aided Modeling Lab
Electronics and Communication Engineering			
III B.Tech – 1st Semester			
1	Analog and Digital Communication Lab	Analog Communication Lab	Digital Circuits Design Lab
III B.Tech – 2nd Semester			
1	Control Systems	Control Systems	Principles of VLSI Design
Computer Science and Engineering			
III B.Tech – 1st Semester			
1	Compiler Design	Compiler Design	Database Management Systems
2	Computer Networks and Compiler Design Lab	Operating Systems and Compiler Design Lab	Database Management Systems Lab
III B.Tech – 2nd Semester			
1	UML and Design Pattern	Object Oriented Analysis and Design	Software Engineering
Information Technology			
III B.Tech – 1st Semester			
1	Software Engineering	Software Engineering	Micro Processors and Micro Controllers
III B.Tech – 2nd Semester			
1	Design & Analysis of Algorithms	Design & Analysis of Algorithms	Python Programming
2	Object Oriented Analysis & Design	Object Oriented Analysis & Design	Unix & Shell Programming
3	Computer Networks	Computer Networks	Web Technologies
4	CN & DM Lab	CN & CT Lab	Web Technologies Lab

(iii) To review and finalize the conduct and evaluation of semester end examinations from the Academic Year 2019-20.

The Member Secretary presented the paper setting and evaluation procedures in semester end examinations. The procedures have been reviewed and approved. The following are the procedures:

1. Question Paper Setting

Question Bank System:

- For each subject controller of examinations shall select *three external paper setters and two internal paper setters* from the panel of paper setters recommended by the Chairman, BoS.
- The paper setters shall prepare the questions from the units specified in the appointment order.
- The Controller of Examinations on receiving the questions from different paper setters will preserve them in the form of a soft copy.

Scrutiny of Question Bank:

- Controller of examinations shall appoint two subject experts, one external expert and one internal expert from the panel of experts recommended by BoS Chairman concerned for each subject to scrutinize the question bank.
- Scrutinizers have to follow the guidelines provided scrupulously.
- Question bank is finalized after scrutiny.
- Question paper is generated at the time of examination from the question bank.
- Detailed key and scheme of evaluation of a subject shall be prepared by internal faculty recommended by the head of the department concerned.

(iv) To take a decision on digital evaluation of semester end examination answer scripts.

The Controller of Examination presented the procedure of digital evaluation of semester end examinations answer scripts. It is resolved to implement digital evaluation in phases to all batches of B.Tech students.

(v) Members suggested to include the courses in curriculum as per the requirements of industry. And also suggested to give more emphasis on practical implementation rather than theoretical content in R20 regulations.

(vi) Member of Academic Council suggested to motivate the students to opt more number of Massive Open Online Courses (MOOCs).